## REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

### I. Disposition of Claims

Claims 1-7 and 9-13 are currently pending in the present application. By way of this reply, claims 6, 7, and 10 have been amended.

### II. Claim Amendments

Claims 6, 7, and 10 have been amended to replace instances of "300mV" to "30mV." This is in accordance with the description of the present invention as recited in lines 10 – 11 on page 4 of the present application. Accordingly, no new matter has been added by way of these amendments.

Claim 7 has been further amended to clarify that at least one of the high-to-low sub-circuit and the low-to-high sub-circuit generates an alarm if a noise error is detected. No new matter has been added by way of this amendment.

### III. Rejection(s) under 35 U.S.C § 102

Claims 1, 2, 4-6, 9, and 10 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,268,635 issued to Bortolini (hereinafter "Bortolini"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a noise margin self-diagnostic receiver circuit. With reference to the exemplary embodiment of the present invention shown in Figure 2 of the present application, a noise margin self-diagnostic receiver circuit includes (i) a comparator **58** for comparing a signal-of-interest **54** to a high reference voltage **vref_H**, (ii) a comparator **60** for comparing the signal-of-interest **54** to a low reference voltage **vref_L**, and (iii) a circuit, formed of flip-flop circuits **62a**, **62b**, **62c**, **62d** and logic gates **64a**, **64b**, **66**, that inputs output signals from the comparators **58**, **60** to determine whether noise error is present on the signal-of-interest **54**. Further, as shown in Figure 2 of the present application, the outputs of comparators **58**, **60** serve as clock inputs to the circuit formed of flip-flop circuits **62a**, **62b**, **62c**, **62d** and logic gates **64a**, **64b**, **66**.

Accordingly, independent claim 1 of the present application requires, in part, that at least one of the high comparator output and the low comparator output ***clocks*** the circuit that processes the high comparator output and the low comparator output. Further, independent claim 9 of the present application requires, in part, (i) activating an alarm if the high signal voltage is less than the high voltage limit, where the activating is dependent on being ***clocked*** by a first signal (generated dependent on comparing a high signal voltage with a high voltage limit) and (ii) activating an alarm if the low signal voltage is greater than the low voltage limit, where the activating is dependent on being ***clocked*** by a second signal (generated dependent on comparing a low signal voltage with a low voltage limit).

Bortolini, in contrast to the present invention, fails at least to disclose the limitations of the claimed invention discussed above. Figure 5 of Bortolini is relied upon by the Examiner as disclosing all the limitations of independent claims 1 and 9 of the

present application. *See* Office Action of September 21, 2004, page 2, paragraph 2. However, the outputs of the purported high comparator **503** and the purported low comparator **504** serve as inputs to a logic gate **505** that outputs to a data input **D** (not to the clock input **CLK**) of flip-flop **506**. Thus, the outputs of the purported high comparator **503** and the purported low comparator **504** ***do not clock*** any circuitry. Accordingly, Bortolini fails to disclose the "clocking" limitations of independent claims 1 and 9 of the present application discussed above.

In view of the above, Bortolini fails to show or suggest the present invention as recited in independent claims 1 and 9 of the present application. Thus, independent claims 1 and 9 of the present application are patentable over Bortolini. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

## IV. Rejection(s) Under 35 U.S.C § 103

Claims 3, 7, and 11-13 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bortolini in view of U.S. Patent No. 5,923,191 issued to Nemetz et al. (hereinafter "Nemetz"). For the reasons set forth below, this rejection is respectfully traversed.

Independent claim 7 of the present application requires, in part, flip-flop circuits that are ***clocked*** by at least one of the output of the high comparator and the output of the low comparator. Further, independent claim 13 of the present application requires, in part, a plurality of flip-flop circuits ***clocked*** by a signal generated dependent on the comparing.

As discussed above, Bortolini fails at least to disclose the "clocking" limitations of the claimed invention. Like Bortolini, Nemetz also fails to at least disclose the "clocking" limitations of the claimed invention. For example, with reference to Figures 4, 5A, and 5B of Nemetz, a reference clock signal **31** serves as (i) a clock input to each of flip-flops **52 – 56** in the high comparator **50** and (ii) a clock input to each of flip-flops **62 – 66** in the low comparator **60**. The output signals **51**, **61** from the high comparator **50** and the low comparator **60**, respectively, ***do not clock*** any circuitry. Further, with reference to Figures 7A and 7B of Nemetz, the output signals **51**, **61** from the high comparator **50** and the low comparator **60**, respectively, serve as data inputs to the logic gates shown in Figure 7B. Thus, the output signals **51**, **61** ***do not clock*** any circuitry. Accordingly, Nemetz fails to disclose the "clocking" limitations of independent claims 7 and 13 of the present application.

In view of the above, Bortolini and Nemetz, whether considered separately or in combination, fail to show or suggest the present invention as recited in independent claims 7 and 13 of the present application. Thus, independent claims 7 and 13 of the present application are patentable over Nemetz. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

## V. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below.

Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 06145.003001; P4928).

Respectfully submitted,

Date: 10/26/04

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